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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/810,005	03/16/2001	Zhongze Wang	303.747US1	7517

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)
	09/810,005	WANG ET AL.
	Examin r	Art Unit
	Samuel A Gebremariam	2811

-- Th MAILING DATE of this communication appears on the c ver sheet with th correspond nc address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48 and 54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-48 and 54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 4, 10, 17, 24, 31, 38 and 45, are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. It is not clear how composite oxidation processing of the gate dielectric turn the gate dielectric layer to a silicon nitride layer. It is widely known that one can possibly form oxynitride layer by the process discussed above.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 5 and 6, are rejected under 35 U.S.C. 102(e) as being anticipated by Yu US patent No. 6,268,253.

Regarding claim 1, Yu teaches a method of reducing a channel length in a transistor, comprising: forming a gate dielectric layer (204) on a semiconductor

substrate (102); coupling a barrier layer (206) to the gate dielectric layer, wherein the barrier layer prevents oxide undergrowth; forming a gate (208) on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and an amount of overlap between the sides of the gate and a pair of source/drain regions (see fig. 7) and oxidizing the gate wherein a portion of the sides of the gate are converted to an oxide (212) and an effective channel length of the gate is reduced (figs. 4 and 5).

Since silicon nitride is a well-known barrier layer, layer (206) inherently prevents oxide undergrowth.

Regarding claim 2, Yu teaches the entire claimed process of claim 1 above including coupling a barrier layer to the gate dielectric layer comprises coupling a silicon nitride (SiN) layer (206) to the gate dielectric layer 204 (fig. 4).

Regarding claims 5 and 6, Yu teaches the entire claimed process of claim 1 above including the gate dielectric layer on a semiconductor substrate comprises forming a gate oxide and gate dielectric layer (204) on a semiconductor substrate (102) (fig. 4).

Claims 7, 8,14, 15,18, 19 and 54 are rejected under 35 U.S.C. 102(b) as being anticipated by Xiang et al. US patent No. 5,866,473.

Regarding claims 7 and 14, Xiang teaches a method of forming transistor, comprising: forming a first source/drain region (212) and a second source/drain region (216) in a semiconductor substrate (204); forming a gate dielectric layer (202) on a semiconductor substrate (204); coupling a barrier layer (206) to the gate dielectric layer,

wherein the barrier layer prevents oxide undergrowth; forming a gate (208) on top of the barrier layer, the gate having sides, and an effective channel length defined by the sides; and oxidizing the gate after all source/drain regions have been formed, wherein a portion of the sides of the gate are converted to an oxide (220) and an effective channel length of the gate is reduced (figs. 2A-2F).

Nitrogen doped layers (210) and (214) form silicon nitride layer that inherently prevent oxide undergrowth.

Regarding claims 8 and 15, Xiang teaches the entire claimed process of claims 7 and 14 above including the coupling barrier layer to the gate dielectric layer comprises coupling silicon nitride to the gate layer.

Regarding claims 11, 12, 18 and 19, Xiang teaches the entire claimed process of claims 7 and 14 above including the gate dielectric layer on a semiconductor substrate comprises forming a gate oxide layer and gate dielectric layer (202) on a semiconductor substrate (204) (col. 2, line 43-61).

Regarding claim 54, Xiang teaches the entire claimed process of claim 7 above including a transistor formed by the method of claim 7 (fig. 2A-2F).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3, is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Gardner et al. US patent No. 6,005,274.

Regarding claim 3, Yu teaches substantially the entire claimed process of claim 1 above except explicitly stating that coupling silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing the gate layer to form a silicon nitride (SiN) layer.

Gardner teaches using remote plasma nitride process to form the gate barrier layer 16 (SiN) (col. 3 line 41-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate remote plasma nitride process taught by Gardner in the method of Yu in order to prevent the migration of undesirable elements from one region of the semiconductor device to other regions.

Claim 4, in so far in compliance with 35 U.S.C 112 and as best understood by the examiner is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu in view of Xiang.

Regarding claim 4, Yu teaches substantially the entire claimed process of claim 1 above except explicitly stating that coupling a silicon nitride layer to the gate dielectric layer comprises composite oxidation processing to form a silicon oxynitride layer.

It is conventional and also taught by Xiang forming silicon oxynitride layer by composite oxidation process of gate dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form silicon oxynitride layer by composite oxidation of the gate dielectric layer in order to form a barrier layer.

Claims 9 and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang in view of Gardner.

Regarding claims 9 and 16, Xiang teaches substantially the entire claimed process of claims 7 and 14 above except explicitly stating that coupling silicon nitride (SiN) layer to the gate dielectric layer comprises remote plasma nitride processing to form a silicon nitride (SiN) layer.

Gardner teaches using remote plasma nitride process to form the gate barrier layer 16 (SiN) (col. 3 line 41-56).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate remote plasma nitride process taught by Gardner in the method of Xiang in order to prevent the migration of undesirable elements from one region of the semiconductor device to other regions.

Claims 21-23, 25, 26-30, 30, 32, 33 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang in view of Gardner.

Regarding claims 21-23, 25, 26, 28-30, 32 and 33, Xiang teaches substantially the entire claimed process of claims 7, 8, 9, 11, 12,14, 18 and 19 above except explicitly stating forming a number of transistors on a semiconductor substrate and electrically connecting the number of transistors.

It is conventional to form more than one transistor and electrically connecting the transistors in a useful MOS device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one transistor and connecting the transistors in order to form a semiconductor device that could be integrated in an IC chip.

Regarding claims 27 and 34, Xiang teaches substantially the entire claimed process of claims 7, 8, 9, 11, 12,14, 18, 19 and 21 above except explicitly stating forming a first source/drain extension adjacent the first source/drain region and a second source/drain extension adjacent the second source/drain region.

It is conventional and also taught by Gardner forming source/drain extension region adjacent source/drain region (fig. 3) (col. 5, line 66-, col. 6, line 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form source/drain extension taught by Gardner in the process of Xiang in order to suppress hot electron effect.

Claims 35-37, 39, 40-44 and 46-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang in view of Gardner and in further view of Sung et al. US patent No. 6,008,085.

Regarding claims 35-37, 39, 40-44, 46-48, Xiang teaches substantially the entire claimed process of claims 7, 14, 21, 27 and 28, above except explicitly stating that the forming a number of word lines coupled to the gates of the number of transistors; and forming a number of bit lines coupled to the first source/drain region of the number of transistors.

Sung teaches word lines (10) coupled to the gates of the number of transistors; and forming a number of bit lines (26) coupled to the source/drain region of the number of transistors (fig. 9).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process of forming a number word lines coupled to the gates of the transistors and forming a number of bit lines connected to the source/drain region taught by Sung in the method of Xiang and Gardner in order to integrate the semiconductor device with other part of an IC chip.

Claims 10, 17, 24, 31, 38 and 45, in so far in compliance with 35 U.S.C 112 and as best understood by the examiner are rejected under 35 U.S.C. 103(a) as being unpatentable over Xiang.

Regarding claims 10, 17, 24, 31, 38 and 45, Xiang teaches substantially the entire claimed process of claim 1 above including coupling a silicon nitride layer to the gate dielectric layer comprises composite oxidation processing to form a silicon oxynitride layer (col. 2, line 43-61).

Response to Arguments

4. Applicant's arguments filed on 8/29/02 have been fully considered but they are not persuasive. Applicant argues that Yu cannot reduce an effective channel length of the gate, because at the time of formation of the removable spacers the effective channel length is not yet defined. Figure 7 of Yu's structure clearly shows that the effective channel length of the gate is reduced and an effective channel length defined

by the sides and an amount of overlap between the sides of the gate and a pair of source/drain regions (230 and 232).

With respect to claims 7-48 and 54 new reference has been used

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4: 30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 305-7646. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
November 15, 2002

TOM THOMAS
SUPERVISORY PATENT EXAMINER
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